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C. Moore

Docket No. 36-0032

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	)	
	)	
Ramon Coronel, et al.	)	
	)	Group Art Unit: 2814
Serial No.: 09/618,708	)	
	)	Examiner: Willie, Douglas A.
Filed: July 18, 2000	)	
	)	
For: LARGE MULTI-FUNCTION INTEGRATED CIRCUIT DEVICE	)	
	)	

CERTIFICATE OF MAILING

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Marilyn L. Beaumont

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APPELLANT'S BRIEF ON APPEAL

Commissioner for Patents
Washington, DC 20231

Sir:

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REAL PARTY IN INTEREST

The application was filed by TRW Inc., which recently transferred title to Northrop Grumman Corporation. The latter named corporation is therefore the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Applicant that will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal.

STATUS OF CLAIMS

Claims 1-40 were originally filed in the application.

Claims 41 and 42 were added during the examination proceedings.

Claims 6-36 and 38-40 were withdrawn from consideration by the Examiner following a four-way restriction requirement as being directed to non-elected inventions. Of the withdrawn claims, claims 8 and 9 were cancelled. Applicant awaits a decision by

the Commissioner of Patents on Applicant's petition to withdraw the restriction requirement and order examination of the withdrawn claims. Applicant's petition asserts that the division requirement lacks a rational basis.

Claims 1-5, 37, 41 and 42 stand rejected following the final examination and are the subject of the present appeal.

STATUS OF AMENDMENTS

No amendment was filed following the final rejection.

SUMMARY OF INVENTION

The concept underlying Applicant's invention is that an electronic system that employs multiple wafers, each containing integrated circuits that provide particular system functions, be formed into a three-dimensional structure, provide wafer-to-wafer communication (and communication with other external devices) by means of an optical data bus and provide a mechanical relationship for the multiple wafers (and external devices) and the optical data bus that permits the disassembly and reassembly of the structure. That is, the invention allows a defective wafer to be disassembled from the structure and replaced; and the three-dimensional structure reassembled. In other words, the structure is repairable[1].

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[1] Modern electronic systems contain separate functional circuit elements, typically fabricated of semiconductor circuits; and those functional circuit elements integrate into a complete system. In some instances, the entire electronic system may be formed as an integrated circuit on a single semiconductor wafer. However, as the size of the system and or number and/or complexity of the functions performed in the system increases, the physical size of the integrated circuit also increases, and may exceed the available space on the largest size commercially available wafer. Thus, more than one wafer is required for such systems. Further, as the size of the integrated circuit and wafer increases, the greater the likelihood that a defect will appear during production that could render a wafer defective. With an increase in defective wafers, production yield of good wafers falls and, conversely, the cost of good wafers necessarily increases, since the good wafers must include the production cost of the bad ones. Further, if the integrated circuit on such wafer fails in service, the entire wafer must be replaced with a like expensive wafer, irrespective of the fact that most of the integrated circuits on the wafer remain good.

To minimize repair cost when an integrated circuit in the electronic system fails, the invention employs a number of individual wafers of smaller size that together define the electronic system, instead of a single large wafer that holds all the integrated circuits; provides wafer-to-wafer communication between the wafers so the wafers may interact when and as required by the electronic system; and physically integrates that communication to allow an individual wafer, such as one that fails in service, to be disassembled from the electronic system and replaced. Since the smaller size wafers are manufactured at higher production yields than a single large wafer, the smaller wafers are significantly less costly per unit to produce. The repair is therefore less costly than the cost of replacement of a much larger size wafer.

Applicant's combination invention includes a number of wafers (12), each physically supporting semiconductor material, the integrated circuits formed in that semiconductor material that perform respective functions required in the electronic system (see application, page 9, lines 2-15) and electrical to optical and optical to electrical converters (see application, page 9, line 22 through page 10, line 7 and Figs. 2a and 2b) defining a node. The wafers are stacked up, one on top of the other, in a three-dimensional structure, but adjacent wafers in the structure are not directly physically attached to each other (see Fig. 5b). As stacked, each wafer presents a node at a predetermined vertical position. Further, the combination includes a straight erect optical data bus that contains reflective gratings at spaced locations along the bus axis for coupling optical data to and from the respective wafers and external devices. The optical data bus is generically denominated 20 and specifically identified as a waveguide 22 (see application, page 10, lines 17-24).

The optical data bus is the straight erect light transmissive waveguide (22, shown in Figs. 5a and 5b), such as a dielectric slab or optical fiber. The reflective gratings (24) are spaced apart along the axis of the optical data bus by the same distance vertically spacing the respective wafers (12). The ends of the optical data bus are located above and below any wafer in the stack (i.e., the bus extends through the front and back sides of the wafer (12) and beyond) and the length of the data bus is greater than the distance between the top surface of the integrated circuits supported on the wafer and the bottom surface of that wafer.

The optical data bus (20, 22, Figs. 2a and 2b) is positioned in optical coupling with the nodes (18) in the wafer, threaded through an opening in each wafer, should the nodes be positioned on the wafer adjacent that opening (see application, page 10, lines 3-5), or orienting the bus alongside the wafers, should the nodes be positioned at the edge of the wafer (application, page 10, lines 5-8). In either embodiment, respective reflective gratings[2] on the bus are aligned with the nodes on respective wafers in the

[2] A Bragg grating is found by Applicant to have the characteristic of diverting a portion of light that propagates along the axis of the data bus to a direction normal to that axis so the light exits from the side of the bus; and, conversely, light incident on the side of the optical bus, such as propagating normal to the bus axis, is received within the optical bus and propagates along the bus axis.

stack for optical communication with the respective converters on the wafer (see Fig. 2b). Light produced by a converter on the wafer is directed to and enters the optical bus from the side. Light propagating along the axis of the optical bus is partially diverted from the side of the optical bus, normal to the axis, and is incident on a converter on the respective wafer.

Given one wafer, the other wafers in the stack are considered "external devices" relative to that one wafer (see application, page 9, lines 12-13 and page 10, lines 14-16), since the wafers are not directly physically attached to one another (see Figs. 2d, 4 and 5b).

When a wafer requires replacement, the wafer may be separated from the combination and a replacement wafer may be easily substituted (see application, page 9, line 20 and page 10, lines 10-14, and Fig. 5a). The achievement provides for a more compact high-speed system assembly that takes advantage of the benefit of optical communications and provides for more convenient disassembly and re-assembly of the system components when repair of a wafer is required.

The restriction requirement in the application was made final. Due to the vagueness of that restriction requirement, the claims under rejection apparently are permitted to recite only a single wafer and "devices" external thereto. Claims that specifically recite a greater of number of stacked wafers, such as appears in claim 19, appear in the non-elected claims that were withdrawn from consideration. Those withdrawn claims may be pursued once Applicant's petition is granted or by filing divisional applications.

ISSUES

(1) Did the Examiner err in rejecting the subject matter defined in claims 1-4, 37 and 41 under 35 U.S.C. §103(a) as being unpatentable over Zavracky et al. (US 5,793,115) in view of Fitch et al. (US 5,612,563) and D'Amato et al. (US 5,511,083)?

(2) Did the Examiner err in rejecting the subject matter defined in claims 5 and 42 under 35 U.S.C. §103(a) as being unpatentable over Zavracky et al. in view of Fitch et al., D'Amato et al. and Tanguay et al. (US 5,568,574)?

GROUPING OF CLAIMS

The claims do not stand or fall together.

ARGUMENT

Applicant believes that independent claims 1 and 37 should be considered separately. The claims contain structural recitations that underlie the feature of repairability of the structure, but expresses that structure in different ways. Considering the vagaries of language and semantics when trying to express something that is new (and the apparent restrictions created by the existing restriction requirement), Applicant remains uncertain as to which claim, if not both, will be perceived by third parties as properly expressing the structural feature of repairability. Applicant is mindful that the existing rules of the Examiner to date permit the Applicant to claim the same invention in different ways as a means to minimize that uncertainty.

Claim 2, depending from claim 1, characterizes a specific embodiment of the invention, reciting the characteristic bidirectionality of the coupler with greater specificity.

Claim 3, depending from claim 2, recites an embodiment in which the coupler equates to a Bragg grating. Claim 4, depending from claim 2, recites an embodiment that contains a plurality of spaced external devices and a like number of couplers. Claim 5, depending from claim 2, recites an embodiment in which the optical data bus is a straight elongate slab of light transmissive dielectric material. Claim 41, depending from claim 3, describes the same additional aspects as claim 4. Claim 42, depending from claim 41, describes the same additional aspects as in claim 5. Each of the dependent claims is believed to recited patentably distinct subject matter.

Independent claim 1 recites "an optical transmission interface extending from the first wafer surface through to said second wafer surface" with an "optical data bus extending through said optical transmission interface" in which the "optical data bus" is "greater in length than the distance between the top of said semiconductor layer and said second surface" and the "first and second ends" (of the optical data bus) "being positioned spaced from said semiconductor layer and from said second surface" and with at least one "external device optically coupled to said optical data bus" and that device being "external to and spaced from said wafer" and with a "node formed on said

semiconductor layer" that contains "means for optically coupling said plurality of integrated circuits and said optical data base through said side of said optical data bus."

The foregoing structure describes not only the optical relationships but the physical relationships that are inherent to having the structure form an assembly that is repairable. That is, the wafer (and/or the external device) can be removed and replaced. Since the prior art does not show or teach such a structure, the claim should be regarded as patentable under 35 U.S.C. §103.

Independent claim 37 recites:

> an optical data bus extending along an edge of said wafer normal to said first wafer surface, and extending beyond both said semiconductor layer and said second surface, said optical data bus having first and second ends and a side and being greater in length that the distance between the top of said semiconductor layer and said second surface;
>
> said optical data bus being physically disconnected from said optical transmission interface and said wafer;
>
> a node formed on said semiconductor layer adjacent to said wafer edge and a side of said optical data bus, said node including means for optically coupling said plurality of integrated circuits and said optical data bus;
>
> said optical data bus including a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of optical energy propagating along said axis of said optical data bus incident thereon to optical energy propagating in a direction normal to said axis out a side of said optical data bus;
>
> one of said plurality of couplers being positioned in alignment with said node; and
>
> the remainder of said plurality of couplers being optically coupled to respective ones of said plurality of external devices.

The foregoing structure recited in claim 37 describes not only the optical relationships but the physical relationships that are inherent to having the structure form an assembly that is repairable and does so in a different manner from claim 1. Since the prior art does not show or teach such a structure, the claim should be regarded as patentable under 35 U.S.C. §103.

Dependent claim 2, dependent on claim 1, defines the invention with greater particularity reciting that the "optical data bus includes a plurality of couplers longitudinally spaced apart along said optical data bus" and that "each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of incident optical energy propagating along said axis of said optical data bus to optical energy propagating in a direction normal to said axis and out said side of said optical data bus." Further, the claim specifies that one coupler is aligned with the node on the wafer and another coupler is optically coupled to the external device.

The foregoing recitation emphasizes the bi-directional nature of transmission to and from the optical data bus defined in parent claim 1.

Claim 3, dependent on claim 2, recites that the coupler is a Bragg diffraction grating. Applicant discovered that the device contains reciprocal properties that are particularly useful in the claimed combination.

Claim 4, also dependent on claim 2, specifies a plurality of devices spaced from one another. The foregoing emphasizes that the combination is unlike the metal via type buses that have devices attached in direct physical contact.

Claim 5, also dependent on claim 2, recites that the optical data bus is a straight elongate slab of optically transmissive dielectric material. The foregoing describes the optical data bus with greater clarity.

Claim 41, dependent on claim 3, contains the same recitation as claim 4, but modifies the combination described by claim 3 with greater specificity.

Claim 42, dependent on claim 41, contains the same recitation as claim 5, but modifies the combination described by claim 41 with greater specificity.

Claims 1-4, 37 and 41 were rejected under 35 U.S.C. §103(a) as being unpatentable over Zavracky et al. in view of Fitch et al. and D'Amato et al. Comments accompanying the final rejection state:

that Zavracky et al. shows a three-dimensional structure, citing Fig. 14 and column 5, line 34, with "SOI structures and show use of fiber optic interconnects (column 12, line 39);"

that Zavracky shows that the couplers extend beyond each level, as is necessary to reach the next level;

that Fitch shows a stacked structure where the stack units are SOS;

that it would have been obvious to replace the SOI with SOS units as a design alternative;

that D'Amato shows the details of a fiber optic coupling which specifically shows a perpendicular fiber mounting with side coupling by means of a grating tap; and

that it would have been obvious to use the D'Amato et al. technique in the Zavracky et al. device to provide details which are not described there.

Dependent claims 5 and 42 were rejected under 35 U.S.C. §103(a) as unpatentable over Zavracky et al. in view of Fitch et al. and D'Amato et al. and further in view of Tanguay, Jr. The comments accompanying the rejection state that the Tanguay patent shows a slab waveguide that uses input/output couplers, specifically making reference to the cover figure and column 5 line 47 et seq. of the patent, and concludes that it would have been obvious to use the slab waveguides of Tanguay in place of the fiber waveguides as a design alternative, "since the slab waveguide structure provides the capability to include other features in the slab substrate such as electro-optic effects which could be used for tailoring the coupling." The foregoing rejection is assumed to include all of the reasoning set forth in the rejection of claims 1 and 37.

In Applicant's opinion, and as the Board will find, the foregoing reasoning contains incorrect factual assertions and ambiguity, and the conclusions of obviousness reached are not supported by the law. Further, the reasoning appears to overlook

express limitations recited in the claims[3]. As a consequence, Applicant brings this appeal.

U.S. 5,793,115 to Zavracky et al. entitled, "Three Dimensional Processor Using Transferred Thin Film Circuits," discloses a multi-layered structure in which separate layers of the semiconductor circuits together define a microprocessor. The layers are fabricated in a separate wafer or thin film material and then are transferred onto the layered structure and electrically and mechanically interconnected in a unitary three-dimensional structure. For example, see the exploded view of Fig. 1 of the Zavracky patent, which shows layer 120 containing certain elements of a digital processor as applied atop another layer 220 of that processor. Inter-layer connections 140, encompassing inter-layer connections 162, 150, 152, 154, 156, 158 and 160.

The detail of the inter-layer connector is illustrated in Fig. 2 of the Zavracky patent. That interconnection is a metal through-hole connections, called vias. See Zavracky, column 7, lines 1-9, which states "An inter-layer connector is illustrated schematically in Fig. 2. Each shift register output is routed to a metal terminal 252. A hole 256 is routed through the second layer exposing a metal path on the first layer. A metal layer 254 is implanted in the hole, providing electrical contact between the terminal 252 on the second crystalline layer and the exposed metal path on the first layer. Interlayer connection is achieved with a minimal loss of die space."

Fig. 14 of the Zavracky patent, which the rejection specifically references, shows a three-layer structure for a three-dimensional computer that incorporates a light emitting diode array 830 located on the uppermost layer 840, which forms an illuminated display. More precisely, referring to the light emitting diodes in that figure, at column 12, line 47, the Zavracky patent states: "In preferred embodiments these LED elements or arrays can be used to form integrated displays or alternatively can be used along with fiber optics to optically interconnect different layers of the structure." As a display, the light emitting diodes in the array may be selectively driven by the drivers 834 and 832 to display the letter "A," for example, or anything else. In Applicant's view, a display is not a "fiber optic interconnect." The alternative specified is impossible to

[3] It is noted that the foregoing reasoning also fails to specifically identify the fiber optic data bus asserted to be "shown" in the principal reference, despite Applicant's request for that information in its reply to the first Office action.

visualize and, Applicant submits, ambiguous. The patent does not explain or show how or what kind of fiber optics may be used with the LED array, or how such fiber optics are able to interconnect different layers and for what purpose. That statement does not indicate whether such fiber optics is to supplant or supplement the existing inter-layer connectors illustrated and described.

The inter-layer connectors are not separately labeled in Fig. 14 of the Zavracky patent. A reasonable presumption is that the inter-layer connectors in Fig. 14 are the same metal vias described in the prior figures.

The description and/or showing made in the Zavracky for the inter-layer connectors, all of which are electrically conductive metal, appear as follows:

(a) In the summary of the invention at column 2, lines 40-67.

(b) In Fig. 2 and the associated description. That interconnection is made by metal through-hole connections, called vias. See Zavracky, column 7, lines 1-9, which states, "An inter-layer connector is illustrated schematically in Fig. 2. Each shift register output is routed to a metal terminal 252. A hole 256 is routed through the second layer exposing a metal path on the first layer. A metal layer 254 is implanted in the hole, providing electrical contact between the terminal 252 on the second crystalline layer and the exposed metal path on the first layer. Interlayer connection is achieved with a minimal loss of die space."

(c) At column 8, lines 20-40, which involves etching and metallization.

(d) At column 13, lines 43-54, which describes the interconnections for the embodiment of Fig. 15, a multi-layer tiling technique, with metal-filled holes formed through a layer.

(e) At column 14, lines 51-63, again describing etching of holes and filling the holes with metal. And

(f) At column 15-lines 8-42.

The text of the Zavracky patent also contains a general statement in the final paragraphs of the Summary section of the specification at column 4, line 7, that refers to inter-layer connections: "Such connections can be optical or electrical, and can run externally or through the bonding layers connecting each layer."

However, there is no illustration of fiber optic interconnections found in the Zavracky patent and/or of any means to access any such fiber optic interconnections and no description of how to make such optical interconnections and employ same in even one of the various embodiments of the Zavracky combination. Applicant disagrees with the statement in the final rejection that the Zavracky patent shows fiber optic interconnects. Applicant invites the Board to inspect column 12, line 39, cited by the Examiner. Applicant submits that no such showing is made or described. Accordingly, Applicant submits that the Zavracky patent does not show[4] fiber optic interconnections.

More specifically, Zavracky does not show or teach, as recited in independent claim 1, "first and second ends" (of the optical data bus) "being positioned spaced from said semiconductor layer and from said second surface" and with at least one "external device optically coupled to said optical data bus" and that device being "external to and spaced from said wafer" and with a "node formed on said semiconductor layer" that contains "means for optically coupling said plurality of integrated circuits and said optical data base through said side of said optical data bus.

Further, Zavracky does not show or teach, as recited in independent claim 37:

> said optical data bus being physically disconnected from said optical transmission interface and said wafer;
>
> a node formed on said semiconductor layer adjacent to said wafer edge and a side of said optical data bus, said node including means for optically coupling said plurality of integrated circuits and said optical data bus;
>
> said optical data bus including a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of optical energy propagating along

[4] Webster's collegiate dictionary: Show, Showing vt 1: to cause or permit to be seen. Show, n 1. a demonstrative display.

said axis of said optical data bus incident thereon to optical energy propagating in a direction normal to said axis out a side of said optical data bus;

Applicant submits that the foregoing statements in the Zavracky patent regarding fiber optics are a teaching that one should try to construct the alternative structure that Zavracky suggests, and not a "showing" as asserted in the rejection.

The cited text in the Zavracky patent appears to imply that fiber optic inter-layer connections are well known and accepted in the multi-layer semiconductor art, without giving any description of the structure. The Examiner appears to accept that implication and, moreover, treats the Zavracky patent as if such optical interconnections are in fact present in the illustrated combinations (e.g., asserting that the Zavracky patent "shows" such optical interconnection), even when those optical interconnections are not in fact present.

When challenged by Applicant to identify and point out such an optical interconnection (as claimed), the Examiner failed to do so. See the penultimate full paragraph on page 9 beginning at line 18 of the amendment filed July 3, 2002. See also the Examiner's comments in paragraphs numbered 12 and 13 of the Final Office action, which Applicant believes to be non-responsive to its request.

In Applicant's view, the statements on fiber optics presented in the Zavracky patent offer merely a gratuitous invitation for those skilled in the art to invent such a structure as an alternative to the metal interconnects described and/or an attempt to ensure that if such an alternative structure is ever invented later by a third party, the alternative structure should be considered to be covered by the patent as an equivalent under any "means" clause found in the patent claims, or under the doctrine of equivalents. Considering the detail with which Zavracky illustrates, presents and describes how to manufacture the electrically conductive metal inter-layer connection, had he been in possession of the knowledge of an optical interconnect system to which Zavracky alludes and/or invented same, reasonable persons skilled in the art would expect that such an optical interconnect would be similarly described in greater detail.

The Zavracky structure is not repairable. That is, the Zavracky structure does not contain structure that permits removal and replacement of a layer of the three-dimensional assembly that is found defective. Each wafer or layer in Zavracky contains through-hole conductors that extend between the front and back sides of the wafer or layer (i.e., through the thickness of the wafer). The through-hole conductors are firmly and directly attached to the wafer (or layer) and the electrical conductor constitutes an electrical data bus through the layer.

An electrical data bus between different layers of the wafer is formed by connecting the ends of the through-hole conductors in series with a conductive epoxy bonding material. Each through-hole conductor then forms a segment of the electrical data bus. The bonding material effectively permanently joins the two layers of the three-dimensional device together. The electrical data bus formed by those serially joined through-hole conductors cannot be separated from those layers and a layer of the three-dimensional assembly cannot be separated without destroying the layers. If one wishes to replace a defective integrated circuit in layer one cannot do so. The entire device must be replaced.

The comments accompanying the final rejection state that the Zavracky et al. structure shows that the couplers extend beyond each level and such extension is necessary to reach the next level. Applicant respectively disagrees. The layers in the device of Zavracky are attached directly to one another in face-to-face contact. The end of a metal via on one layer butts (and is bonded to) the end of another metal via in the underlying layer aligned therewith to provide a conductive path between. Thus, the ends of the metal vias are not spaced from each side of the wafer.

The secondary patent to Fitch et al., U.S. 5,612,563 entitled, "Vertically Stacked Vertical Transistors Used to form Vertical Logic Gate Structures," illustrates logic gates that are formed of three transistors that are fabricated and physically attached together in a vertically stacked unitary assembly. Those transistors are formed on a silicon substrate. The stacked relationship allows the logic gate to occupy a smaller area. The Fitch patent appears to be cited in the rejection for the limited purpose of showing that SOS semiconductors were known previously, whereas Zavracky employs SOI structures. It is noted that the transistors are permanently joined together in the layered

structure and, should one of the transistors fail in service, the resultant structure is not repairable. The Fitch patent, thus, does not appear to merit further detailed discussion.

NO MOTIVE OR INCENTIVE IS IDENTIFIED BY THE PATENT OFFICE TO EXPLAIN WHY ONE WHO IS GIVEN THE DEVICES OF THE ZAVRACKY PATENT WOULD BE IMPELLED TO INCORPORATE AN SOS TYPE SEMICONDUCTOR FOR THE SOI STRUCTURES DISCLOSED IN ZAVRACKY.

U.S. 5,511,083 to D'Amato et al. entitled, "Polarized Fiber Laser Source," describes a laser (10) constructed of an optical fiber (12). The optical fiber contains two Bragg gratings (14, 16) embedded at spaced locations along the axis and an internal region located between those gratings that is doped with a rare earth dopant and functions as a laser cavity. The laser is optically pumped by light applied to the grating (14) at one end of the optical fiber (12). The pumping light is supplied by pumping light source (22). A grating tap (26) is written into the optical fiber at a location inside the formed laser cavity between the two gratings (14, 16) earlier mentioned.

Coherent light generated by the lasing action of the optical fiber laser normally contains light of two different polarizations, referred to as "s" and "p" polarizations. D'Amato's structure employs grating tap 26 to filter out light of the undesired polarization, the "s" polarization, by shunting light of that polarization (as may have been reflected back from output grating 16) in a direction normal to the axis of the laser cavity (and out the side of the fiber laser), whereby that light is discarded. As a result, light of the "s" polarization that is reflected toward the input grating (14) is diverted and any of that "s" polarized light not so diverted is insufficient in quantity to sustain lasing. As a result, the laser of D'Amato is able to sustain lasing for "p" polarized light and emits only "p" polarized coherent light.

D'Amato et al. discovered that a Bragg grating 26 passes light of the "s" polarization to a greater extent than light of the "p" polarization and D'Amato employs that effect to produce a laser that emits only "p" polarization from the output window of the laser. By judicious design the grating tap 26 is designed to shunt sufficient quanta of the "s" polarized light from propagating along the axis of fiber optic to reduce the amount reflected back to the reflective input grating (window) to a level below the

amount necessary to sustain lasing, while allowing sufficient "p" polarized light to pass and sustain lasing at the "p" polarization.

The comments accompanying the final rejection state that "D'Amato et al. shows the details of a fiber optic coupling which specifically shows a perpendicular fiber mounting with side coupling by means of a grating tap (see cover Figure and abstract)."

Applicant submits that the foregoing statement as best understood is incorrect. All of the elements in the D'Amato structure are mounted coaxially. There is no perpendicular fiber mounting, and there is no perpendicular fiber mounting with side coupling by means of a grating tap. The only light coupled to the laser is light 20 that is applied to the input end of the fiber optic laser 10. The "s" polarized light, indicated at 34, that is shunted (e.g., "coupled-out") is diverted by grating 26 (and is effectively discarded). Therefore, the shunted "s" polarized light is not coupled to anything.

The D'Amato et al. patent does not show or describe the use of a Bragg grating to couple light into the optic fiber from the side, such as is employed in Applicant's claimed invention, for bidirectional transmission along the axis of the optic fiber.

NO MOTIVE OR INCENTIVE IS IDENTIFIED BY THE PATENT OFFICE TO EXPLAIN WHY ONE WHO PLANS TO CONSTRUCT AN OPTICAL DATA BUS FOR WAFER TO WAFER COMMUNICATION WOULD REFER TO THE ART OF LASER LIGHT SOURCES FOR THE STRUCTURE OF AN OPTICAL DATA BUS.

The first full paragraph on page 11 of Applicant's amendment dated July 3, 2002 points out that none of the references cited in the first Office action contained "light coupled to and from the side of the optical fiber." In response, the Examiner dropped the reference to Van Zeghbroeck (paragraph 14 of the Final Office action) and substituted the patent to D'Amato et al. (paragraph 7 of the Final Office action). Then the comments accompanying the final rejection state that the grating couplers (i.e., the grating couplers in the D'Amato et al. patent) "obviously will couple light both into and out of the fiber." Certainly with the hindsight gleaned from Applicant's specification and extracting the grating and fiber optic components from the laser of D'Amato, the Examiner's statement concerning the D'Amato patent is true. But that mode of operation of the grating is not shown or taught in the D'Amato patent.

D'Amato does not show or teach that his grating tap 26 couples light into the fiber for bi-directional transmission along the fiber. Implicitly, the Examiner concedes that omission. The Examiner fails to point out the basis for his statement that the grating used in D'Amato is capable of coupling light into and out or a fiber, which, Applicant believes to be based on the teachings of the Applicant's specification. Applicant submits that the foregoing reasoning demonstrates an unsuccessful attempt at piecemeal reconstruction of the claimed invention based solely on hindsight.

More importantly, APPLICANT SUBMITS THAT THE D'AMATO ET AL. PATENT IS NON-ANALOGOUS ART AND, AS SUCH, SHOULD BE WITHDRAWN FROM CONSIDERATION.

The D'Amato patent is in a different field of endeavor from the present invention. D'Amato describes a polarized laser and is classified in class 385/14. The present invention is an integrated circuit device and is classified in class 257/83. Further, even the non-elected claims in the present application were classified in accordance with the restriction requirement (see Office action dated Jan. 20, 2002) as falling within classes 259/237, 359/118, and 257/777. Thus, the D'Amato patent is different in subject matter from anything claimed in the present application under the classification standards used by the U.S. Patent and Trademark Office.

The present invention relates to an integrated circuit device having multiple wafers (and/or a wafer and at least one external device) in which the device includes optical communication between wafers and/or wafer and an external device and the integrated circuit device can be disassembled and reassembled to replace a wafer that is found defective. D'Amato does not relate to any of those subjects.

In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned. See Wang Laboratories, Inc. *v.* Toshiba Corp. 26 USPQ2d 1767 (Fed. Cir. 1993); *In re* Oetiker, 24 USPQ2d 1443 (Fed. Cir. 1992).

A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it

deals, logically would have commended itself to an inventor's attention in considering his problem. *In re* Clay 23 USPQ2d 1048, 1060-61 (Fed. Circ. 1992).

The D'Amato patent fails to satisfy any of the foregoing criteria. Applicant submits that the burden of demonstrating that a prior patent constitutes analogous prior art lies with the Examiner. Should the Examiner fail in that burden, the reference is non-analogous prior art and must be withdrawn from consideration in any evaluation of patentability under 35 U.S.C. §103. And if the non-analogous art was necessary for the Examiner to make a *prima facie* case of obviousness of the claimed invention, then that determination of obviousness under 35 U.S.C. §103 also fails. Since the claims are not obvious, the claims should be allowed.

The patent to Tanguay et al., U.S. 5,568,574, granted Oct. 22, 1996 entitled, "Modulator-Based Photonic Chip-to-Chip interconnections For Dense Three-Dimensional Multichip Module Integration," unlike the principal reference to Zavracky et al., does show optical interconnections between adjacent layers. That interconnection is either planar or volume diffractive optical elements that are proximity coupled to the active layers (column 5, line 41-column 6, line 8). And the communication is one-way. The device includes a source of optical power (light) from source 18 that is redirected by grating 26 (e.g., split, fanned-out in a direction perpendicular to the original propagation path) into a plurality of channels to produce a series of light sources in parallel. The divided light power is directed to individual rib or channel waveguides formed on substrate 22. In turn, those waveguides contain outcoupling gratings, for example, 16a and 16b, which direct the incident light perpendicular to the surface to transmissive light modulators, as illustrated in Fig. 3. Presumably, the electronically controlled light modulators in the Tanguay patent, which respectively modulate the light supplied by the light power bus, are respectively modulated with some kind of information, whether digital or analog is unclear. In that sense, the layers of light transmissive material between layers may be considered an optical data bus. All of those layers are permanently bonded together.

The rejection asserts that the Tanguay patent shows a slab waveguide using grating input/output couplers and makes reference to the cover figure and column 5, line 47, et seq., of the patent. The rejection then concludes that it is obvious to use the slab

waveguides of Tanguay in place of the fiber waveguides as a design alternative, since, the Examiner hypothesizes, "the slab waveguide structure provides the capability to include other features in the slab substrate such as electo-optic effects which could be used for tailoring the coupling."

Applicant finds the foregoing factual assertions and reasoning unintelligible. The cover figure is taken from Fig. 3 of the Tanguay patent. That drawing figure is described at column 8, line 48 through column 9, line 20. Elements 30a and 30b are transmissive light modulators located on modulator array substrate 31. Elements16a and 16a are individual outcoupling gratings arranged on the surface of an optical power bus 10. The modulator array substrate 31 is bonded to optical power bus 10.

The Tanguay patent does not describe the gratings 16a and 16b as being input/output couplers as asserted in the rejection. On the contrary, those gratings are described only as output couplers (*sic*, outcoupling gratings). Further, the rejection does not identify the so-called slab waveguide the Examiner finds in the figure in the Tanguay patent, but not apparent to Applicant. Could the Examiner be referring to the large number of rib or channel waveguides 28 (formed in substrate 22 on the power bus 10) in the optical power distribution network of Fig. 2?

Nor does the rejection identify or point out the fiber waveguides that are to be replaced by any such slab waveguides. Since the principal reference, Zavracky et al., does not show any fiber waveguides, the rejection cannot be referring to that patent. Applicant is guessing that any so-called slab waveguide is to replace the fiber waveguide found in the laser of the secondary reference to D'Amato. Perhaps that reconstruction of the D'Amato laser might be possible, although Applicant is unable to understand how or why.

Lastly, Applicant is unable to understand the Examiner's conjecture as to the motivation for such a change. The recited motivation appears contrived. Applicant does not understand what electro-optic effects can be included on the so-called slab for "tailoring the coupling" that cannot be included in a fiber waveguide.

In evaluating patentability under 35 U.S.C. §103, an Examiner must determine whether the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

The prior art references that show or teach a three-dimensional structure do not permit disassembly and replacement of a wafer (or layer) from the structure. The layers are permanently bonded together and cannot be separated without destroying one or more layers. The rejected claims each recite an aspect of the structure that is characteristic of a three-dimensional structure in which a wafer may be disassembled from the structure and replaced. The recited aspect is not shown or taught by any of the references, whether taken singularly or together in any combination. Since those aspects are not shown or taught in the references, Applicant submits the claimed invention cannot be considered obvious under 35 U.S.C. §103.

Applicant submits that the Examiner is attempting to piece together the claimed invention from the prior art, and is unsuccessful at that. As pointed out, the cited prior art does not show or teach all of the claim limitations (even if the non-analogous art of D'Angelo were accepted as being analogous art). The prior art does not show or teach having the optical data bus being unconnected to the wafer (as in claim 37) and does not show or teach having the ends of the straight optical bus (e.g., the waveguide) spaced from the top and bottom surface of the wafer (as recited in claim 1). The prior art cited by Examiner is intended to show what was known to those of ordinary skill in the art. Thus, from the state of that prior art, the limitations set forth in the claims were unknown to those of ordinary skill. If unknown, the difference could not have been obvious.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re* Vaeck, 20 USPQ2d 1438 (Fed. Cir. 1991) and Manual of Patent Examining Procedure, Section 2143. As discussed, this last requirement is clearly lacking. For that reason alone, the Examiner has not made a *prima facie* case of obviousness.

In re Fritch, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992), this Board made clear that the Examiner bears the burden of establishing obviousness under 35 U.S.C. §103 and reaffirmed longstanding law in making clear what the Examiner cannot do to establish the obviousness of a claimed invention.

As stated in the Fritch decision (at 1783), "The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art (citing *In re* Piasecki 223 USPQ 785, 787-88 (Fed. Cir. 1984). That burden can be satisfied only '... by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art that would lead that individual to combine the relevant teachings of the references'" (citing *In re* Fine, 5 USPQ 2d, 1596, 1598 (Fed. Cir. 1988). The patent Applicant may then attack the Examiner's *prima facie* determination as improperly made out, or the Applicant may present objective evidence tending to support a conclusion of nonobviousness (citing *In re* Heldt 167 USPQ 676, 678 (CCPA 1970).

(at page 1783) Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so (citing ACS Hosp. Systems, Inc. *v.* Montefiore Hosp, 221 USPQ 929, 933 (Fed. Cir. 1984). Although couched in terms of combining teaching found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification (citing *In re* Gordon 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious (citing *In re* Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). This court previously stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention" (citing *In re* Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)).

Applicant submits that the Examiner failed in the burden of presenting a *prima facie* case of obviousness. Applicant maintains that there is no teaching, suggestion or incentive in the prior art to modify or combine the teachings of the prior art in the manner suggested by the Examiner (to the extent the Examiner's suggestions can be understood). The Examiner's proposed modifications of the principal reference are based in great part, if not entirely, on hindsight. As also revealed, even with those hindsight modifications, the Examiner was unable to reconstruct the claimed invention.

Accordingly, Applicant respectfully requests this honorable Board to reverse the rejection of the claims.

The attached appendix contains a copy of the claims involved in this Appeal.

Respectfully submitted,

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APPENDIX TO THE APPLICANT'S BRIEF ON APPEAL

1. An integrated circuit device comprising:

a wafer having a first surface, a second surface opposite said first surface and an optical transmission interface extending from said first wafer surface through to said second wafer surface;

a semiconductor layer disposed on said first wafer surface;

a plurality of integrated circuits formed on said semiconductor layer;

an optical data bus extending through said optical transmission interface normal to said first wafer surface, said optical data bus having first and second ends and being greater in length that the distance between the top of said semiconductor layer and said second surface, said optical data bus extending beyond both said semiconductor layer and said second surface with said first and second ends being positioned spaced from said semiconductor layer and from said second surface;

at least one device optically coupled to said optical data bus, said at least one device being external to and spaced from said wafer; and

a node formed on said semiconductor layer adjacent to said optical transmission interface and a side of said optical data bus, said node having means for optically coupling said plurality of integrated circuits and said optical data bus through said side of said optical data bus for providing optical data communication with said at least one device.

2. An integrated circuit device as recited in claim 1, wherein said optical data bus includes a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a

direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of incident optical energy propagating along said axis of said optical data bus to optical energy propagating in a direction normal to said axis and out said side of said optical data bus;

one of said plurality of couplers being positioned in alignment with said node on said wafer; and

at least one other of said plurality of couplers being optically coupled to said at least one device.

3. An integrated circuit device as recited in claim 2, wherein each of said couplers comprise a Bragg diffraction grating.

4. An integrated circuit device as recited in claim 2, wherein said at least one device comprises a plurality of devices, each of said devices being spaced from one another along said optical data bus, and wherein each of said plurality of said couplers of said optical data bus are positioned adjacent a respective one of said plurality of devices.

5. An integrated circuit device as recited in claim 2, wherein said optical data bus comprises a slab of light transmissive dielectric material, said slab having a straight elongate geometry.

37. An integrated circuit device comprising:

a wafer having a first surface, and a second surface opposite said first surface;

a semiconductor layer disposed on said first wafer surface;

a plurality of integrated circuits formed on said semiconductor layer;

an optical data bus extending along an edge of said wafer normal to said first wafer surface, and extending beyond both said semiconductor layer and said second surface, said optical data bus having first and second ends and a side and being greater in length that the distance between the top of said semiconductor layer and said second surface;

said optical data bus being physically disconnected from said optical transmission interface and said wafer;

a plurality of external devices coupled to said optical data bus; and

a node formed on said semiconductor layer adjacent to said wafer edge and a side of said optical data bus, said node including means for optically coupling said plurality of integrated circuits and said optical data bus;

said optical data bus including a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of optical energy propagating along said axis of said optical data bus incident thereon to optical energy propagating in a direction normal to said axis out a side of said optical data bus;

one of said plurality of couplers being positioned in alignment with said node; and

the remainder of said plurality of couplers being optically coupled to respective ones of said plurality of external devices.

41. An integrated circuit device as recited in claim 3, wherein said at least one device comprises a plurality of devices, each of said devices being spaced from one

another along said optical data bus, and wherein each of said plurality of said couplers of said optical data bus are positioned adjacent a respective one of said plurality of devices.

42. An integrated circuit device as recited in claim 41, wherein said optical data bus comprises a slab of light transmissive dielectric material, said slab having a straight elongate geometry.